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Challenges in nanoelectronics

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Abstract. The size of electronic devices has been decreasing to nanometer size regime which requires quantum mechanics to understand its operation and optimization. Many features associated with quantum effects are not all desirable from the engineering point of view: the charging of a nano-capacitor runs into Coulomb blockade; the dielectric constants of nanoparticles is much reduced; the binding energy of the shallow dopants in a nanoscale quantum dots becomes many times of $k_B T$ resulting in intrinsic behavior regardless of doping density; etc. There are other serious problems preventing the implementation of redundancy and robustness which are so essential to the electronic devices, for example, inadvertent defects cannot be avoided; contacts and input/output have to be sufficiently small resulting in pushing beyond the frontier of lithography. This article aims to discuss some of the fundamental points still requiring better understanding, and what lies ahead in future nanoelectronics.

Introduction

Professor Kroemer at the Nobel lectures during the APS March Meeting said that: "You notice the old figures of heterostructures that I showed with rounded profiles without scales, it is because I did not know how sharp are the band-edge offsets, nor how large are the offsets". This sentence points to the relative roles of understanding versus technological advances. We all agree that ideas and understandings are crucial to new technologies, however it is the steadfast advancement of technology that brought mankind to what we have today. Traditionally, machines help us to tilt and rearrange our land for farming and control of our habitat, but now, computers are extending our brain. We are expanding our reach as well as accelerating our control of nature. In what follows some are fundamental physics and engineering details while others are based on my personal assessment. For example, only devices like detectors may be operated at low temperatures whereas memory devices should not be operated at low temperatures, and the steady march toward ever decreasing size of integrated circuits (ICs) is based on ever refinement of nano-lithography. Another point is that quantum wells (QW) are far more likely to be incorporated into ICs than quantum dots (QD) because contacts for QW is planar while it is necessary to use quantum wires for QD.

Tunneling time in a quantum well

Several approaches [1, 2] were used: (a) solving the time dependent Schroedinger equation with prescribed initial conditions, and (b) specifying a wave-packet and calculating the time it takes to traverse the double barrier structure [2]. Results show that the tunneling time of a Gaussian packet from the time-dependent solution is very close to the phase-delay time $\tau = d\phi/d\omega$, where $\phi = kd + \theta$, is the total phase shift, with θ being the phase of the transmission coefficient, and d , the length of the double barrier (DB) structure. Resonance is produced by a wave bouncing back and forth for a number of cycles determined by the quality factor of the resonant system.

The tunneling time given by the time for a Gaussian wave-packet traverses the structure using the time dependent Schrödinger equation gives essentially the same result [3]. Since the thesis [2] is not readily available, several salient features of this work are highlighted here. First, the Green's function for the one dimensional equation for the double barrier (DB) structure is obtained. Excitation functions are chosen for various cases: specifying a spatial distribution at $t = 0$, or specifying a time function (usually a pulse at a given energy between $t = 0$ to T) at a given location such as $x = 0$, or $x = \text{center of the well}$, etc. Laplace transform is then used. The inverse transforms give the desired results. If one wants to calculate the charge inside the well at any given time for a particular distribution, it would be necessary to multiply $Q(t)$ for the charge by $n(\omega) - n'(\omega)$ and integrate over all ω , with n and n' given by the distribution functions on the inside and transmitted side of the DB respectively. $Q(t)$ confined within the system is obtained as a function of time by integrating $|\psi(t)|^2$ over both the well and the barrier regions.

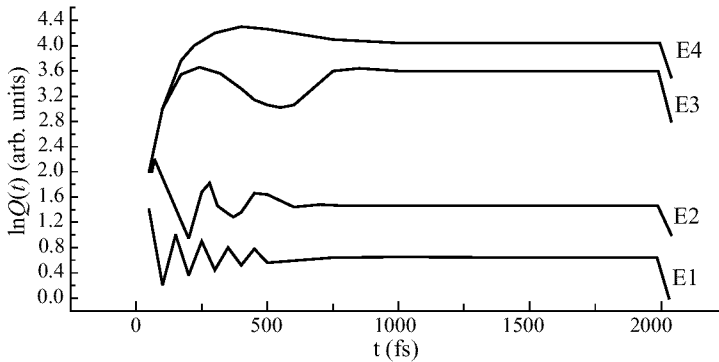


Fig. 1.

Figure 1 shows the charge inside the quantum well for an incident wave at energy E and duration 2 ps. The top curve E4 is at $E = 0.068$ eV, the energy at resonance for a DB structure of barrier width 2.5 nm and GaAs well width of 6nm, and a barrier height of 0.3 eV. Note that at energies away from the resonance, (E3, E2 and E1=0.079, 0.05 and 0.03 eV), oscillation of $Q(t)$ is very strong during the build-up time, while it is more monotonic at resonance. However, the decay is always monotonic. Instead of specifying the initial condition at the left side of the DB structure, we have also studied the build-up time and decay time for an excitation $\exp(-i\omega t)$ at a point within the well and calculate the steady state wave-packet. To our surprise, as the point of excitation moves towards the center of the well from the edge of the barrier, the resonance behavior gradually disappears. The details of those cases are not quite the same. Precise results do depend on the form of the excitation. Although in all cases tunneling does slow down near resonance. The delay time at resonance calculated from $\tau d_0 / (\hbar k / 2m^*) (E / \Delta E)$ with E and ΔE being the energy and linewidth is so close to the solution for Gaussian packet. Although tunneling time slows down near resonance, at the first resonance, it is still less than one quarter of a ps, and 25 fs near the second resonance. An ideal resonant tunneling device is very fast.

Coulomb blockade and quantum of conductance G_0

Conductance for a device, in this case a QD, connected to two leads at very low temperature exhibits equally spaced steps of $G_0 = e^2/h$ versus voltage [4]. The discrete steps originate from the discrete nature of the electronic charge. The applied voltage needs to increase in

steps of e/C to overcome the Coulomb potential of the charging of a capacity C , known as Coulomb Blockade [5, 6]. Typically for a QD of dimension $2\text{ nm} \times 2\text{ nm}$, the electrostatic energy is $\sim 10\text{ mV}$ so that discrete steps in conductance may be observed at low temperatures. It is important to note that C is not a constant because each additional charge introduced into the dot, the additional electron interacts with the electrons already present in a complicated manner to be discussed in the next section. There is another far more important point to be stressed here, i.e. all the work thus far involves adding an additional electron to the dot as a time independent before and after description. To understand device performance such as the charging speed, it is necessary to employ the time-dependent Schrödinger equation. Oscillations again will occur, as the tunneling case presented, for G_0 , $2G_0$, etc. The physics is same as the charging of a capacitor where oscillation depends on the length of the transmission line used in bringing in the charge.

Capacitance of a nanoscale sphere

A classical capacitor stores charges, and the electrostatic energy is the only energy stored. However, electrons have kinetic energy as standing waves confined inside a quantum well or quantum dot. We have calculated the quantum mechanical capacitance of a small sphere from the definition $E_2 - E_1 = e^2/2C_{\text{eff}}$, where E_1 and E_2 are the one- and two-electron ground state of the quantum dot [7]. The effective capacitance may also be defined in terms of $E_3 - E_2$ and so on. Since the added electron needs to interact with two electrons present in the dot, the effective capacitance will not be a constant with respect to the number of electrons already present in the dot. Quantum mechanically, it is somewhat similar to the difference between the He atom and hydrogen atom, only that the calculation is quite complex because it is necessary to include the electron-electron interaction together with the induced image-charge and their interactions. We were surprised that even the classical electrostatic calculation of the capacitance taking into account all the interactions of electron-electron and their images, have not been calculated [7]. These interactions lowers the total energy of the systems inside a capacitor, resulting in a deviation from the classical capacitance. The quantum mechanical calculation includes the kinetic energy, thus drastically reduce the capacitance at nanoscale regime.

Since we assumed that the coherence length of the electron wave function is only 12 nm , it is expected that C_{eff} at 12 nm approaches the 'classical' value (including all the e-e interactions), $\sim 10^{-18}$ to 10^{-19} F , we found that at 6 nm and 3 nm , C_{eff} is only one-half and one-third as large as the classical values, respectively. Likharev used a constant value for the capacitance in his Hamiltonian because the size of the quantum dot is quite large in his case [6]. The kinetic energy of an electron is inversely proportional to the square of the dimension of confinement, which grows faster than the Coulomb energies. Consequently, C_{eff} decreases when the ground state energies dominates over the electrostatic energies. Not only that this C_{eff} should be used in nanoscale modeling, it should be possible to tailor-made capacitor in a nano-composite.

Dielectric constant and doping of a nanoscale silicon particle

Reduction of the static dielectric constant becomes significant as the size of the quantum confined systems, such as quantum dots and wires, approaches the nanometric range. A reduced static dielectric constant increases Coulomb interaction energy in quantum confined structures. The increase of the exciton binding energy significantly modifies the optical properties, and the increase of the shallow impurity binding energy may profoundly alter the transport, i.e., resulting in an intrinsic conduction even with doping. The dielectric constant

$\varepsilon(a)$ was first derived using a modified Penn model taking into account the eigenstates of a sphere instead of the usual free electron energy-momentum relation [8–10]. The size-dependent $\varepsilon(a)$ is given by [10]

$$\varepsilon(a) = 1 + (\varepsilon_B - 1)/[1 + (\Delta E/E_g)^2] \quad \text{and} \quad \Delta E = \pi E_F/(k_F a),$$

where E_F and k_F are the energy and k vector at the Fermi level with the total number of the valence electrons, and E_g is taken as 4 eV, the center of the ε_2 versus energy for silicon. For a 1 nm QD, $\varepsilon(a)$ is reduced to half the value. The formula is easily applicable to a number of situation in nanoscale modeling. For example, the binding energy of dopants of a nanodot [11], estimating the breakdown voltage of ultra-thin oxide, and in Coulomb blockade. The dielectric mismatch between the media results in induced charges at the interface. We found that these induced effects are as important as the dielectric constant effect. There are many such induced terms: in addition to the direct Coulomb term, there are the self-polarization between the electron and its image; the term between the electron and the induced polarization of the donor. Since both the self-polarization and induced-polarization terms depend on $\varepsilon_1 - \varepsilon_2$, with 1 and 2 for the nanoparticle and the matrix respectively, the binding energy can be strongly affected by the sign of $\varepsilon_1 - \varepsilon_2$. For vacuum, at a radius of 2 nm, the binding energy is 0.8 eV resulting in no extrinsic conduction at room temperature. Immersing in water, the binding energy is reduced to 0.1 eV, allowing some extrinsic conduction at room temperature. Since doping is essential to the operation of semiconductor devices, and the trend of ever reducing the device size, the mechanism of extrinsic conduction governed by the size forms an important issue in modeling.

Tunneling via nanoscale silicon particles

Nicollian and I reasoned that if we could make the particles small enough, confinement would increase the energy separation to values allowing resonant tunneling at room temperature. A diode structure was fabricated with nanoparticles of silicon, $\sim 4\text{--}8$ nm, embedded in an oxide matrix [12, 13]. Sharp conductance peaks were observed at reverse bias between 10–11 V. Resonant tunneling diode, RTD gives current peaks whenever the energy of the incident electron coincides with the eigenstates of the quantum system [14]. Using a metal contact having a large Fermi energy, current steps instead of peaks should result at resonant. We found that the conductance peaks appear near 10–11 V reverse bias, and steps appear above 20 volts bias, with a pronounced hysteresis shift of ~ 7 mV [15, 3]. The details are quite complicated. Some salient features are summarized below:

1. The linewidth of the conductance peaks $\sim k_B T$.
2. The QD energies are much greater than the Coulomb energy for the size under consideration. Therefore we observed two groups of closely spaced current steps separated by the separation of the E_1 and E_2 quantum states of the dot [16, 17].
3. With large metal contacts, conductance is proportional to the density of states, giving rise to conductance peaks for 3D and steps for 1D structures. (We think that some of the particles are coupled to form 1D structures.)
4. Hysteresis is present in most cases particularly noticeable at higher bias, but not always.

5. We observed oscillation in time due to negative resistance resulted from e-h pair production by hot electrons injected into the substrate [17, 18].
6. What we have learned is that devices with large contact covering many QDs is unlikely to play a role in future devices. Significant progress in nanostructure devices must wait for the improvement in lithography allowing contacting a single QD. Although we thought about a multifunctional device, but not really seriously! See Ref. [18] for a summary of this work.

A new type of superlattice: semiconductor-atomic superlattice (SAS)

Conventional superlattices are formed with repeating a basic period consisting of a heterojunction between two materials [19]. A new type of superlattice are formed by replacing the heterojunction between adjacent semiconductors with semiconductor layers separated by adsorbed species such as oxygen atoms; and CO, molecules, etc. [20, 21]. This new type of superlattice, SAS, semiconductor-atomic-superlattice, fabricated epitaxially, enriches the present class of heterojunction superlattices and quantum wells for quantum devices. The Si growth beyond the adsorbed monolayer of oxygen is epitaxial with fairly low defect density. At present, such a structure shows stable electroluminescence and insulating behavior, useful for optoelectronic and SOI (silicon-on-insulator) applications. SAS may form the basis of future all silicon ‘superchip’ with both electrons and photons. Without a strong optical transition, silicon has not played a role in optoelectronic technologies such as injection lasers and light emitting diodes. Superlattices and related quantum wells have been developed into the mainstream of research and development in semiconductor physics and devices primarily with III–V and II–VI compound semiconductors. Silicon dioxide with a barrier height of 3.2 eV in the conduction band of silicon is amorphous, preventing the building of a quantum well structure on top of the a-SiO₂ barrier. Several years ago, it was proposed that the oxides of one or two monolayers might allow the continuation of epitaxy [23]. Our growth beyond a barrier structure consisting of 1 or 2 nm of silicon sandwiched between adjacent layers of adsorbed oxygen up to 50 Langmuirs of exposure for each layer is epitaxial and low in stacking faults as determined in high resolution X-TEM. We have presented high resolution TEM in both cross-section and plane-view [22]. The measured barrier height is ~ 0.5 eV [24]. Using an assumption that in the SAS structure, the amount of electron transfer from the Si to O is only half as much as SiO₂, the maximum barrier height is estimated at 1.5 eV instead of 3.2 eV [25]. Following the observation of visible luminescence in nanoscale silicon particles [26], we have observed stable electroluminescence in the visible spectrum of a 9-period SAS structures [27]. With partially transparent Au electrode, the emitted light is green. The spectrum extends well into the blue region of the visible spectrum. The defect density is below 10^9 cm⁻². We have lowered the defects by almost two orders of magnitude during the past couple of years. Thus we are optimistic that further reduction should be possible. Note that the defect density in Si/a-SiO₂ interface is generally much higher.

We have also fabricated a 9-period Si/O superlattice for possible replacement of SOI (silicon-on-insulator). Preliminary results show the structure is epitaxial with insulating behavior. With similarly doped silicon, a decrease in current of five orders of magnitude at the same applied voltage of several volts has been observed.

What we have demonstrated is that silicon can grow epitaxially beyond adsorbed atomic or molecular species, resulting in a new kind of superlattice. We want to emphasize that it is important to have the silicon layer having at least several atomic layers. Otherwise, the

structure becomes similar to the ALE, atomic layer epitaxy, which is entirely different from the SAS. In SAS, the adsorbed oxygen monolayers are constrained by the Si surfaces on both sides, whereas, in ALE, there is nothing to prevent silicon and oxygen atoms forming a specific crystalline structure, or an alloy structure. It is the constraint imposed by the silicon surfaces that gives rise to the superlattice structure, exhibiting the physical characteristics reported here. As we have shown that SAS, or SMS (M for molecular) indeed constitutes a new type of superlattice. It is hopeful that the reported EL and PL can allow applications in optoelectronic devices, and the reported epitaxially grown SOI can replace the present SOI for quantum devices, such as 3D ICs.

To Summarize, 1D quantum confinement will dominate future devices because of the planar nature of the contacts for input/output. Any 3D nanostructures will have to wait for further improvement in nano-lithography.

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